REMARKS

This amendment is in response to the Office Action dated May 15, 2006. Claims 1-20 are pending. Claims 1, 2, 8 and 15 are currently amended to further clarify the invention. Applicants respectfully request reconsideration of the application in view of the following remarks submitted in support thereof.

Rejections under 35 U.S.C. § 102:

Claims 1-6, and 14-20 were rejected under 102(b) as being anticipated by U.S. Patent Application No. 5,822,599 to Narayan et al. This rejection is respectfully traversed.

Narayan discloses a microprocessor including a plurality of decode units configured to detect double dispatch instructions and dispatch these instructions to decode units. The more complex instructions are executed by an MROM unit in a serial fashion. The complex instructions are detected prior to decode and dispatched to the MROM unit.

The Examiner asserts that Narayan discloses the feature of circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access of an operand from a memory location. In support of this assertion the Examiner refers to the main memory or the data cache of Figure 2. Applicants respectfully disagree with this assertion and submit that neither the Examiner nor Narayan specifies what the circuitry enables a single cycle access of an operand from memory. Applicants respectfully request that the Examiner specify where Narayan discloses any circuitry enabling a single cycle access, i.e., where the operand can be addressed and operated on in a single clock cycle (see the present application page 17, lines 21-23 for the definition of single cycle access, which is further specified in amended claim 2). If the Examiner is referring to memory or data cache 224 as having circuitry enabling a single cycle access, Applicants respectfully request that the Examiner specify where this feature is

specified as nowhere in Narayan is this capability discussed. Furthermore, as stated in column 66, lines 22-25, an extra clock cycle is needed for decoding instructions having more than 4 prefix bytes. Even if there was only one clock cycle used to decode the prefix byte, because the operand still needs to be operated on.

The Examiner further states that the feature of circuitry for aligning operands to be processed by the ALU, the circuitry for aligning operands causing the operands to be aligned by a lowest significant bit, wherein the circuitry for aligning the operands supplies an extension to the operands to allow the ALU to process different size operands is taught in column 17, lines 32-42. Applicants respectfully request that the Examiner explain how a prefix designating the bit size of the operand discloses aligning operands by a lowest significant bit. First of all the prefix deals with a single operand and nowhere is it mentioned that multiple operands are aligned by a lowest significant bit. The decoding process referred to by the Examiner is for determining the size of the operand to determine where to route the operand and for complex instructions (see column 16). Furthermore, the Applicants would like for the examiner to explain how the prefixes for multiple operands would be aligned as nowhere is this mentioned is Narayan. Accordingly, claims 1-6 are allowable for at least these reasons.

Claim 14 includes the features of a read only memory (ROM), the ROM configured to store code common to each processing stage associated with a pipeline of processors and a code RAM configured to download code specific to the processing stage and wherein the code specific to the processing stage is enabled for single cycle access. The Examiner never provides any analysis of where Narayan teaches a ROM configured to store code common to each processing stage associated with a pipeline of processors. Narayan does not have a pipeline of processors and is silent as to this feature. Applicants respectfully request that the Examiner address this feature or withdraw this rejection. The Examiner further asserts that

the MROM unit of Narayan discloses the code RAM. As the MROM unit of Narayan breaks down complex instruction to simpler instruction, the Applicants submit that the MROM unit is a processor and not a memory unit (see column 3, lines 45-65, and column 6, lines 20-30). In addition, as specified in claim 14, the code RAM and the ROM are part of the fetch and decode circuitry. The examiner is asserting that a portion of the main memory and the MROM unit is includes in the fetch and decode circuitry and refers to Figure 2 of Narayan. As illustrated in Figure 2, the MROM unit and the Main memory are different blocks and the main memory is not even in communication with the early decode units or the MROM. Applicants respectfully request that the Examiner specify what basis there is for classifying the MROM and a portion of the main memory as fetch and decode circuitry. Claim 14 further includes the feature of align function circuitry for aligning the first and the second operands to be processed by the ALU, the align function circuitry the circuitry causing the first and the second operands to be aligned by a lowest significant bit, wherein the align function circuitry supplies an extension to the each of the operands to allow the ALU to transparently process different size operands. As discussed above, Narayan is silent as to aligning two operands and the Examiner has not provided any analysis on where multiple operands are aligned according to the lowest significant bits. In addition, the prefix codes of Narayan are for determining where to route the operands and not placing extensions on the operands. Accordingly, claims 14-20 are allowable for at least these reasons.

Rejections under 35 U.S.C. § 103:

Claims 7-13 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Narayan. This rejection is respectfully traversed. Claim 7 includes the features of circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access from a memory location. As mentioned above, Narayan is incapable of enabling a single cycle access. In addition the

Examiner asserts that the feature of an arithmetic logic unit (ALU), the ALU configured to receive a first and a second operand; the second operand being specified from an internal register, the first operand having a mask enabling the ALU to process a non-masked segment of the first operand. The Applicants respectfully disagree with this characterization. First of all, the Examiner states that the functional units of Figure 33 include the ALU, then the Examiner states that REGF is the internal register of the ALU. In Figure 33 REGF is external to the ALU. Applicants respectfully request that the Examiner specify the basis for modifying the external REGF to be internal to the ALU if this rejection is maintained in light of the minimal discussion of Figure 33 in the specification. The Examiner admits that Narayan does not teach the first operand having a mask. However, according to the Examiner, one skilled in the art would have looked to column 144 and saw a mask was applied to status bits that ensure that write back destinations are not the same, when the status bits are set for destinations of different size. Applicants disagree with this assertion as applying a mask to status bits for a write back interface provides motivation for applying a mask to one of two operands for processing by an ALU. As Narayan never discusses processing two operands at a time one skilled in the art would not have modified Narayan as suggested by the Examiner. Applicants would like to additionally point out that the LIL and NC status bits must be checked and reset and this would require an extra clock cycle, further supporting that Narayan is incapable of performing a single access cycle as specified in claim 7. Accordingly, claims 7-13 are allowable over the cited reference.

A Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6921. If any other fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP223). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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